ELECTRONIC DEVICE USING CARBON NANOTUBES

The invention relates to an electronic device incorporating a tubular shaped carbonmolecule supported by a substrate, which molecule is provided with source and drain electrodes, and a gate electrode.

5   Such an electronic device is known from Nature, Volume 393, May 7, 1998, pages 15 to 17. From this publication a transistor is known having a so called semi-conducting carbon nanotube of about 1 nanometer in diameter that bridges source and drain electrodes. A gating voltage is applied to the

10   silicon substrate that supports the carbon nanotube in order to induce carriers onto the nanotube to control the transistor.

When more than one or even many nanotube electronics are to be implemented on a silicon substrate the challenge

15   then is to be able to control the respective transistors individually. It is therefore a prime objective of the invention to provide an electronic device according to the preamble of the main claim that is capable of being controlled individually.

20   A further objective is to provide such an electronic device having a gain of substantially more than one.

The electronic device according to the invention is therefore characterised in that the gate electrode is a metallic electrode. The metallic electrode in turn is prefera-

25   bly supported by the substrate.

Preferably the metallic electrode has a surface layer of oxide thus preventing short circuiting the source and drain electrodes. Native oxide provides an effective insulation layer with respect to both the carbon molecule per

30   se and the respective source and drain electrodes. The oxide layer can also be grown for instance by evaporation, but should remain thin.

Particularly good results can be achieved when the metallic electrode is selected from the group consisting of

35   aluminium, zinc and copper. Preferably however the metallic electrode is an aluminium electrod .

The invention will now be further elucidated with reference to the drawing.

In the drawing:

- fig. 1 shows a side view at the lay-out of an electronic
5   device according to the invention;

- fig. 2 shows I-V characteristics of a single nanotube transistor according to the invention;

- fig. 3 shows several electronic devices according to the invention incorporating 1, 2 or 3 transistors.

10   Referring now first to fig. 1, a schematic device lay-out of an electronic device according to the invention is shown. The device 1 incorporates a tubular shaped carbon molecule 2 which is supported by an aluminium wire 3 which, at the side facing the tubular carbon molecule 2, is provided
15   with an insulating native Al_2O_3 layer 3'. On both its extremities the tubular carbon molecule 2 is contacted by gold contacts 4 and 5 which are acting as the source and drain electrode respectively. The thickness of the Al_2O_3 layer 3' on the surface of the aluminium electrode 3 is in the order of mag-
20   nitude of a few nanometers and much shorter than the separation between the contact electrodes 4 and 5 which is approximately 100 nanometer. This provides an excellent capacitive coupling between the gate electrode 3 and the tubular carbon molecule. This construction of the electronic device accord-
25   ing to the invention allows for the integration of multiple similar devices acting as (nanotube) field effect transistors on the same substrate 6 whereby each transistor is individually controllable.

Fig. 2 shows the device characteristics of a typical
30   nanotube FET. The variation of the current I through the device as a function of the gate voltage V_g (Fig. 2a) shows that very significant doping can be achieved. Starting with negative V_g, the current first decreases, then becomes immeasurably small, and finally increases again. This indicates that V_g
35   shifts the Fermi level successively from the valence band (accumulation regime) to the gap (depletion) and finally to the conduction band (inversion) of the semi conducting nanotube. The nearby Al gate thus makes it possible to change the

doping of the nanotube over the full range from p-doping to n-doping. Several volts can be applied on the gate without destroying the oxide layer. This is quite remarkable since the insulator layer is only a few nanometers thin, and it in-
5 dicates the excellent quality of the gate oxide. The break-down threshold voltage where the layer is destroyed is typi-cally between 2 and 5 V. A small gate leakage current (a few pA) is observed for V_g approaching such large gate voltages.

Fig. 2b shows the current versus bias voltage char-
10 acteristics. Typical FET-type curves are found. For small source-drain voltages, the current changes rapidly then when the source-drain voltage V_{sd} is made more negative. This is called the linear regime because the current is proportional to V_{sd}. When V_{sd} becomes more negative than $V_g - V_t$, the current
15 through the transistor changes more gradually (the saturation regime). Here V_t is called the threshold voltage at which (some) current starts to flow. It has a value of about -1.0 V for the transistor to which Fig. 2b relates. For a constant source-drain voltage in the saturation regime, the current
20 has a parabolic dependence on the gate voltage I ~ $(V_g-V_t)^2$. This data shows that the transconductance of the nanotube transistors is 0.4μSiemens and the on/off ratio is at least 10^5. The maximum current that the nanotube transistor could tolerate was in the order of 100 nA and the on resistance was
25 about R_{sd} = 33 MΩ for V_{sd}= -1.0 V, V_g = -1.3 V. Note that it is clear from Fig. 2a that even lower resistances can be achieved upon using higher gate voltages (80 kΩ for V_g = -3 V). A voltage gain of at least 10 can be achieved.

Fig. 3a shows the input-output characteristics of an
30 inverter constructed from a nanotube transistor and an off-chip 100MΩ bias resistor. An inverter is a basic logic ele-ment that converts a logical 0 into a logical 1, and a logi-cal 1 into a logical 0. When the input is a logical 1 (V_{in} = 0 V), then the nanotube is non conducting and the output is
35 pulled to -1.5V, representing a logical 1.

The output voltage of an inverter should make a rapid transition from one logic level to the other as the gate voltage is swept. In this device according to the inven-

tion, the output voltage changes three times faster than the input voltage in the transition region indicating that this particular device has a voltage gain of 3 (other devices showed a gain of up to 6).

5   A NOR gate can be constructed by simply replacing the single transistor in the inverter with two transistors in parallel as shown in Fig. 3b. When either or both of the inputs are a logical 1 (V_{in} = -1.5 V), at least one of the nanotubes is conducting and the output is pulled to 0 V (logi-

10   cal 0). The output is a logical 1 only when both inputs are a logical 0 so that neither nanotube is conducting.

In Fig. 3b, the output voltage is plotted as a function of the four possible input states (0,0), (0,1), (1,0) and (1,1), verifying that this circuit indeed operates as a

15   NOR gate. Using variations of the device circuitry one can realise any logical gate in this way.

A flip-flop memory element (SRAM) was constructed from two inverters, see Fig. 3c. When the output of each inverter is connected to the input of the other inverter, two

20   different stable states are possible: The outputs can either take on the values (1,0) or (0,1). A logical 1 is written into memory by forcing the circuit into the (0,1) state and a logical 0 is written by forcing the circuit into the (1,0) state. To test the working of the memory cell, a volt-

25   age source was attached to one input and a logical 0 was written to V_{out} by driving V_{in} to -1.5 V. The switch was then opened again and the memory cell maintained a logical 1 at the output. These data thus demonstrate the stable memory function of a 2-transistor nanotube circuit according to the

30   invention.

A 3-transistor device was realised in the ring oscillator shown in Fig. 3d. This circuit, used to generate an oscillating ac voltage signal, was built by connecting three inverters in a ring. A ring oscillator has no statically sta-

35   ble solution and the voltage at the output of each inverter consequently oscillates as a function of time. One of the inverter outputs is plotted in Fig. 3d. A clear voltage oscillation is observed. The 5 Hz frequency of the oscillations

is determined by the output impedance of the inverters (~1 GΩ) and the capacitance of the output nodes which currently is dominated by the ~100 pF parasitic capacitance of the wires connecting to the off-chip bias resistors.

5   A method to manufacture an electronic device according to the invention is explained below.

Al gates 3 for multiple nanotube transistors are first patterned using electron beam lithography on an oxidised Si wafer 6. During evaporation, the sample was cooled

10 to liquid nitrogen temperature in order to minimise the roughness of the Al surface 3. The insulator layer 3' consists of the native oxide that grows by exposing the Al surface 3 to air. The precise thickness of this layer is in the order of a few nanometers. Carbon nanotubes 2 produced by laser ablation

15 are dispersed on the wafer 6 from a dispersion in dichloroethane. Using an atomic force microscopy, those nanotubes 2 are selected that have a diameter of about 1 nm and that are situated on top of the Al gate wires 3. Their co-ordinates are registered with respect to alignment markers. Finally, con-

20 tact electrodes 4,5 are fabricated with electron-beam lithography by evaporating Au directly on the nanotube 2 without adhesion layer.